Quick Start for Signal Integrity Design Using Agilent ADS

Number One in a Series of Ebooks from Agilent EEsof EDA

by Sanjeev Gupta and Colin Warwick, Agilent Technologies

Test Drive Advanced Design System Today!

- Are you a signal integrity engineer?
- Heard about ADS but haven't used it yet?
- Want a quick way to try it out for yourself?

Great, we created this e-book for you! It shows you how to drive ADS and gives you a glimpse of some of its features and their benefits.

Sanjeev Gupta

Colin Warwick

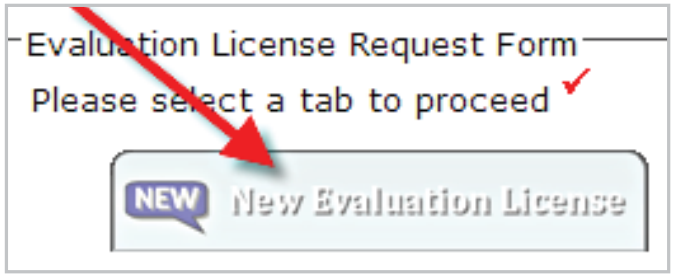
Agilent Technologies

Let's get started!

First, request an evaluation license at this link:

http://eval.soco.agilent.com/onlineevals/faces/home.jsp?prodfam=SIVT&cmpid=34689

- Click on the "New Evaluation License" tab:

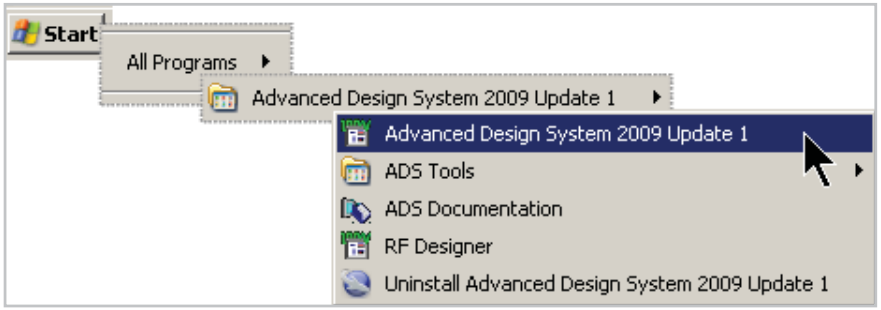


- Send in the completed form.
- Download the installation zip file for your operating system from: **http://www.agilent.com/find/eesof-ads-latest-downloads**
- Unzip into a fresh folder, say, C:\ads_cdimage\ .
- Inside that folder double click on setup.exe and follow the instructions given by the installer.

Below, we'll assume Windows ® and a default installation folder C:\ADS2009U1\ .

When you receive your license file (license.lic):

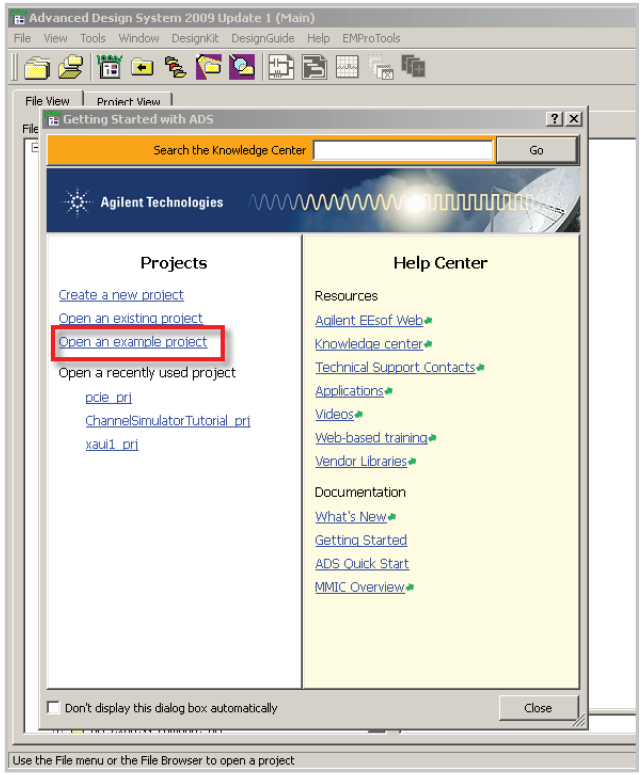
- Save a copy to the folder C:\ADS2009U1\licenses .
- From the Start menu, start ADS:



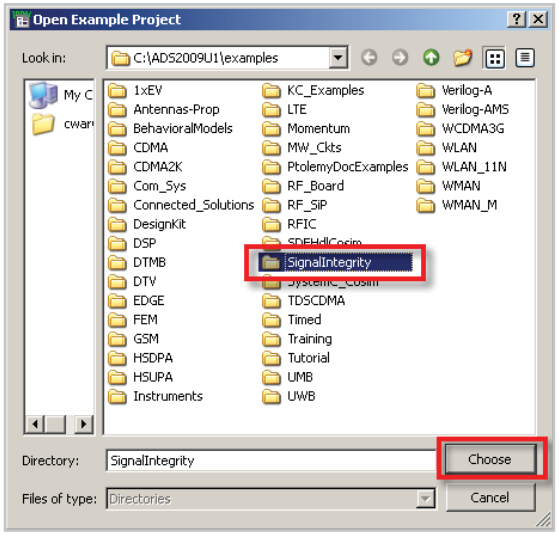
A First Look at ADS Using an Example Project

After the splash screen, the Main ADS window appears with the '*Getting Started with ADS*' window over it. This has several Help Center links on the right, but since you'll be following this guide, skip those for now. Instead:

- Click the *Open an example project* link:

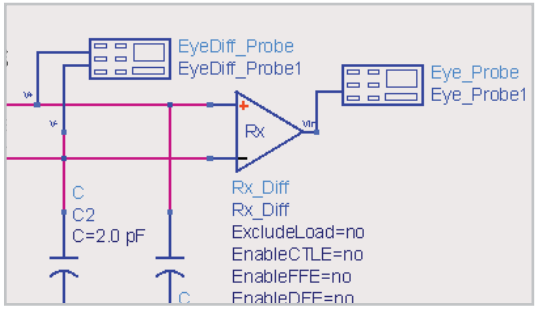


- Choose or double click the SignalIntegrity folder.
- Don't double click, but use the Choose button to select the ChannelSimulator-PCIe2_prj project. (If you do double click, you'll push down into the project hierarchy instead of choosing the project. If so, back out and use the Choose button.)



The schematic window named A_Readme.dsn opens.

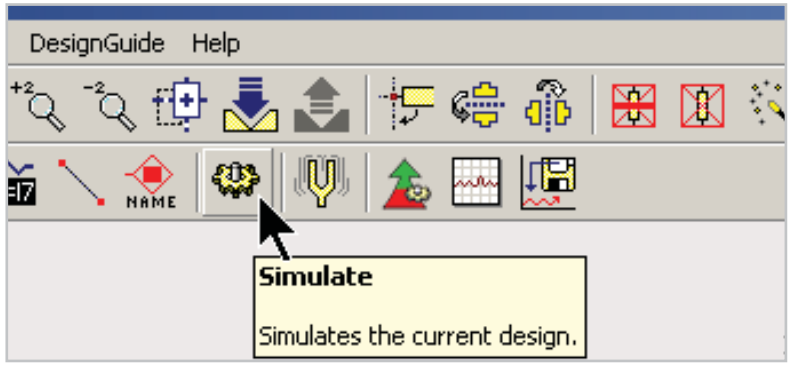
- From the menu bar of this window, select *File* ▶ *Open Design...* ▶ PCIe_channel_4.dsn
- In this Open Design dialog box, click OK.



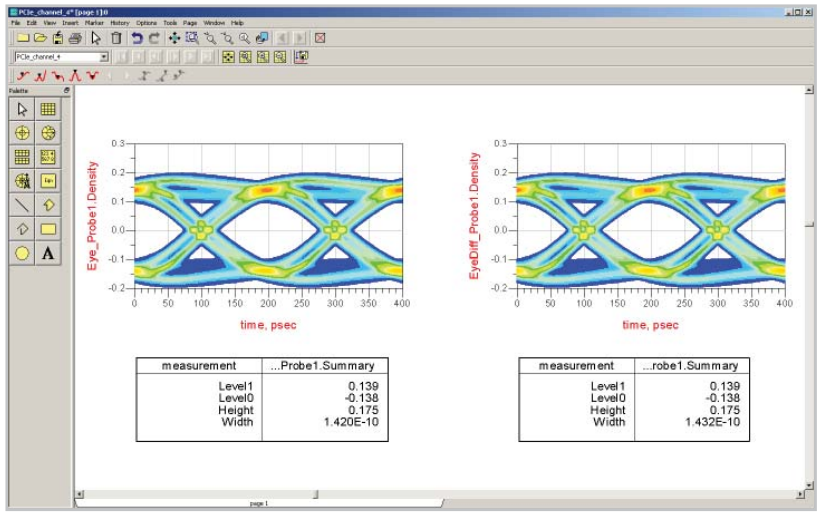
The schematic (a PCI Express design) opens. Note that the components *EyeDiff_Probe1* and *Eye_Probe1* are collecting data before and after the receiver component, *Rx_Diff*.

Simulate the Example Schematic

In the tool bar of this schematic window, click on the Simulate icon:

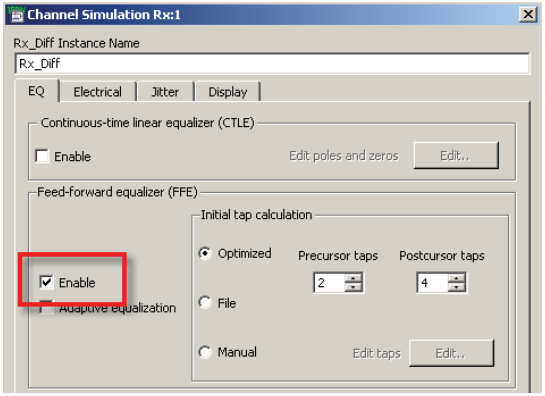


First the status window opens with some warnings (ignore these for now), then messages about simulation progress, then after a minute or so the data display opens:



The before and after eye diagrams are nearly identical because the receiver equalization is turned off.

- Back in the schematic, double click on the *Rx_Diff* component to open its dialog box.
- Enable the Feed-forward equalizer:



- Click OK to dismiss the dialog box.
- *Simulate*. 

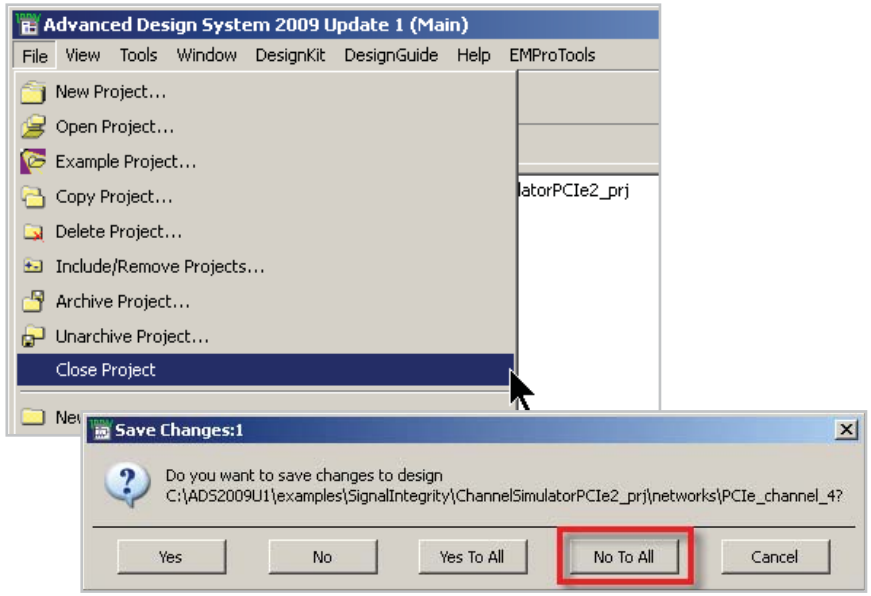
After completion, the data display window updates.

Note the improvement in post-receiver eye height and width:

measurement	...Probe1.Summary
Level1	0.133
Level0	-0.131
Height	0.199
Width	1.492E-10

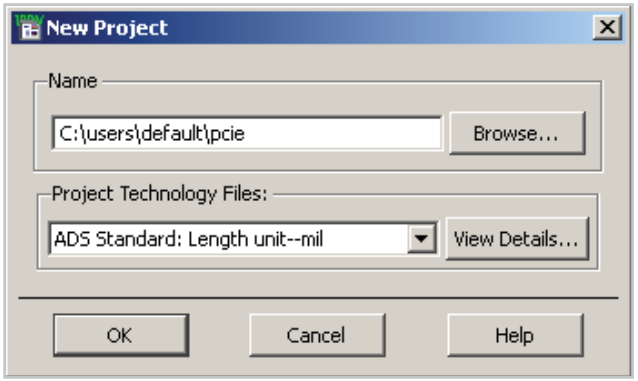
Start a New Project

- Switch to the ADS Main window
- Close the example project by selecting *File* ▶ *Close Project:*

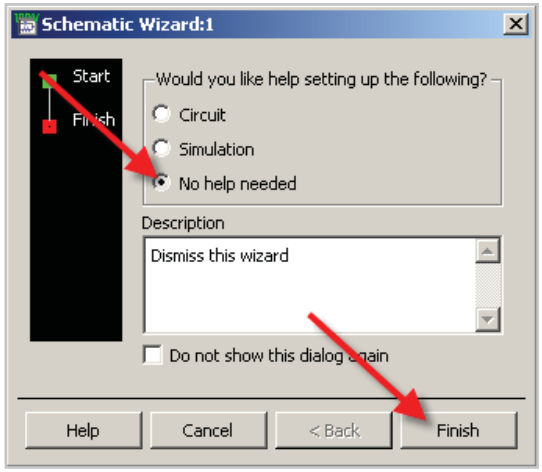


- Start a new project by selecting *File* ▶ *New Project*... from the Main ADS window.

- The *New Project* dialog box appears:
- Enter: C:\users\default\pcie in the Name field.
- Click OK.
- ADS appends _prj to the project folder name. By default, the *Schematic Wizard* appears, but skip it for now and follow this guide instead.



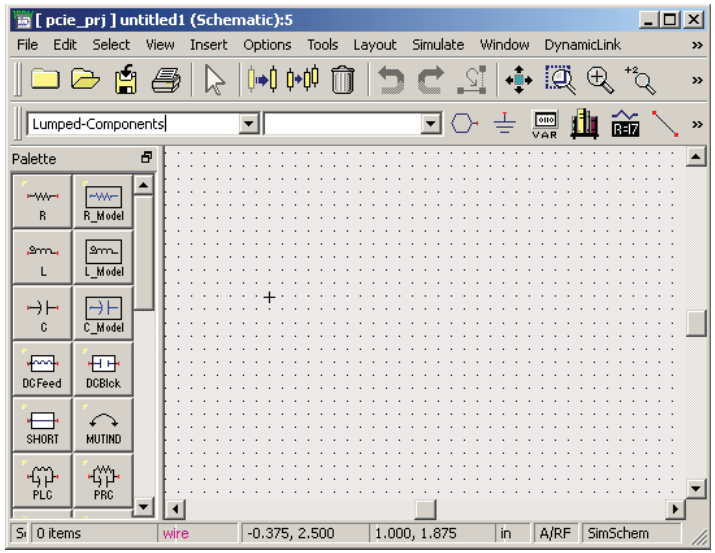
- In the Schematic Wizard dialog box, select the *No help needed* radio button.



- Click on the *Finish* button to dismiss the Wizard.

Overview: The ABCs of ADS

A blank schematic window appears:



From this point, there are only three steps between you and answers you need in ADS. We call them:

The A B C 's of ADS

Schematic *Simulation* *Data*

In a nutshell:

A) Place components, connection lines (called nodes), and simulation controller onto the schematic. (The icon for schematic is  . Later, we'll explore the option to associate layout artwork with a schematic. The layout icon is  .)

B) Create a dataset by clicking on the "run simulation" icon:  .

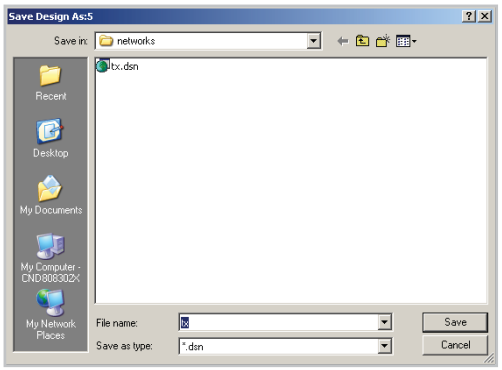
C) Create a data display to view your results in. The icon for the data display is  .

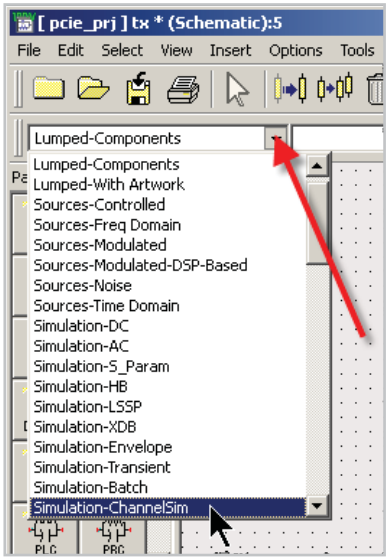
That's it! That's all there is to it!

The ABCs will quickly become second nature to you. But for this first pass, let's walk through each one in detail by building a simple design to look at the eye diagram that we will be transmitting later on.

A. Place Components and Simulation Info on Schematic

- Select *File* ▶ *Save Design As*... from the Schematic menu bar. The *Save Design As* dialog box appears:
- Enter tx as the File Name. ADS appends .dsn to the file name.
- Click the Save button. ADS saves the schematic in the networks subfolder of your project folder pcie_prj. Save early, save often.





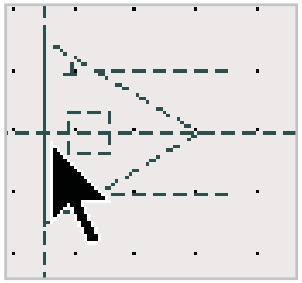
Mirroring the real world, there are thousands of components available in the ADS library  .

The *palette* on the left of the schematic is a tool to help organize them. By default, the *Lumped-Components* palette is displayed.

- Click on the arrow to show the list of available palettes.
- Select *Simulation-ChanSim.*

- Click on the *Diff Tx* (differential transmitter) icon 

.
- The cursor becomes a crosshairs with a ghostly image of the component:



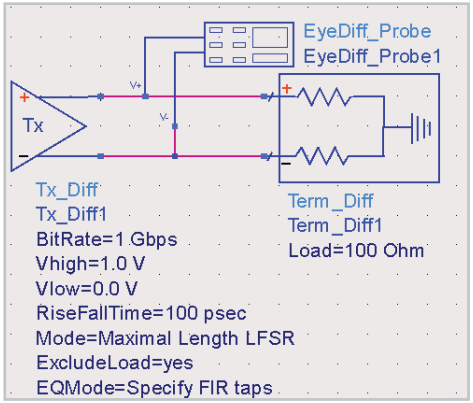
- Click on the blank canvas to place the transmitter.
- The ghost image remains, so cancel out of the command by pressing the *Esc* key or clicking on the *End Command* icon  .
- Pick the Diff Term (differential termination) icon and place it to the right of the transmitter.

Some components are used so much they live not in a palette but on the toolbar, e.g. Wire and Ground.

- Pick the Wire icon:  .
- Join the + and – nodes to + and – , respectively. The red dot turns blue to indicate connection has been made.

A (cont.): Complete the Schematic

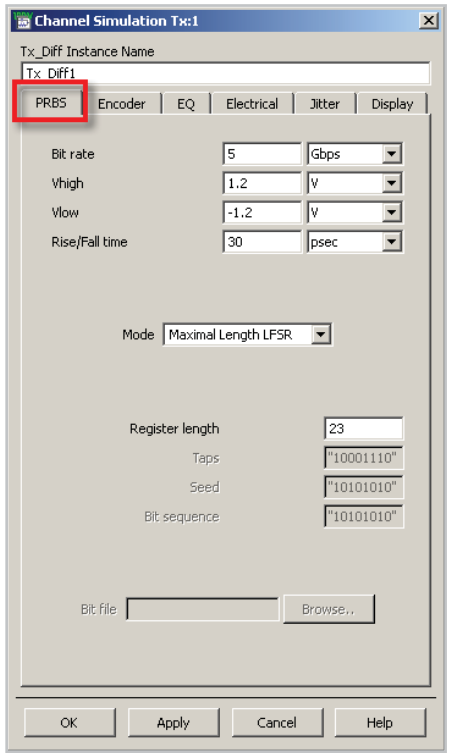
- Pick and place the *EyeDiff_Probe* (differential eye probe) like so: 



Any time you make a mistake, you can simply click on the undo button  on the tool bar. If you change your mind, you can undo the undoing by clicking on the redo button  .

You can set up the parameters of a given component instance directly on the schematic or via its dialog box. We'll use the latter method for now.

- Double click on the Tx_Diff1 instance to open its dialog box.



On the PRBS tab set:

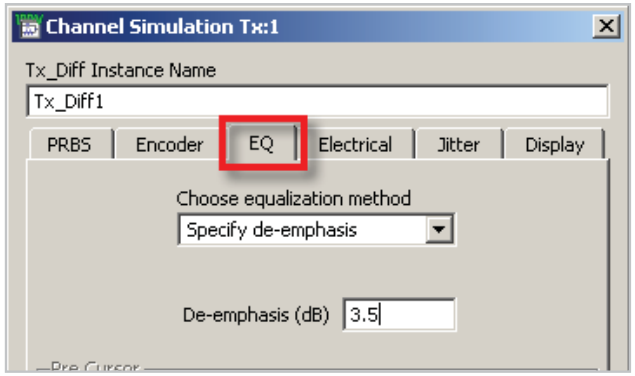
- Set *Bit Rate* = 5 Gbps
- *Vhigh* = 1.2 V
- *Vlow* = –1.2 V
- *Rise/Fall Time* = 30 ps
- *Register Length* = 23

Click on the *Help* button to bring up the doc page for the component.

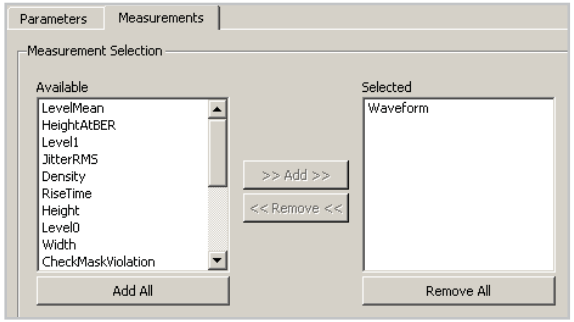
The documentation pages contain a wealth of information about the parameters and algorithms used.

A: Set Component Parameters, (Continued)
B: Simulation Controller and Simulation,
C: Data Display

- On the *Encoder* tab set the encoding to *8B10B*.
- On the *EQ* tab, set *Choose equalization method* to *Specific de-emphasis* and set *De-emphasis* as a positive quantity.



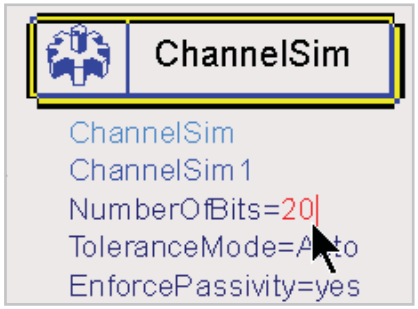
- Click OK to dismiss *Tx_Diff1*.
- Double click on *EyeDiff_Probe1*.
- In its dialog box, set the *Data rate* to 5 Gbps.
- Click on the *Measurement tab*, *>> Remove >>* the default measurements, *>> Add >>* *Waveform* instead.



Step B: Simulation Controller and Simulation

- Click on the Channel Simulator icon 

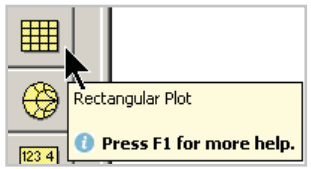
.
- Drop the controller onto the schematic, then hit *Esc* to *End Command.*
- Edit *NumberOfBits* to 20, by directly clicking on the schematic.
- Click away to finish editing.
- On the schematic toolbar, click on *Simulate*  .

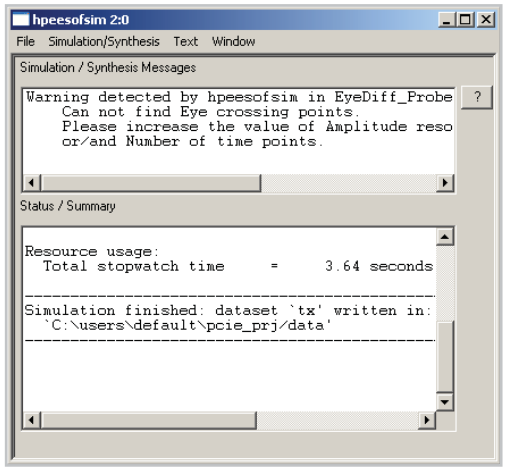


Again the status window opens, the simulation runs in a few seconds, and then the data display window opens.

Step C: Data display

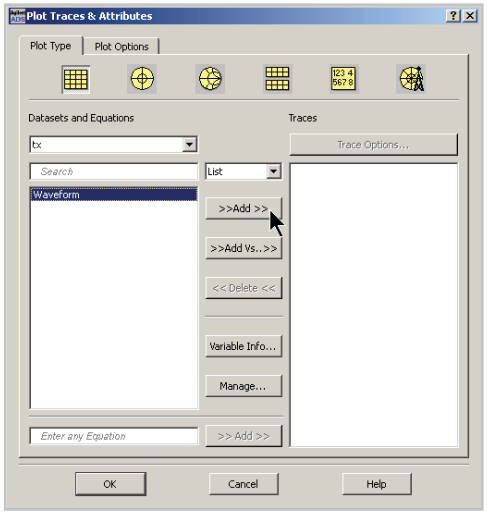
- In the palette, click on the Rectangular Plot icon and drop a blank plot onto the display area.





C: Data Display (Continued)

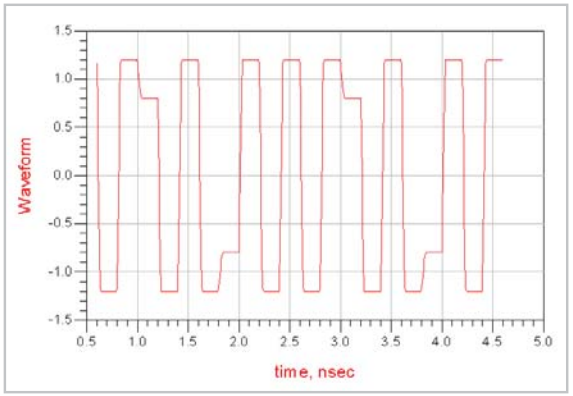
When you drop a fresh plot onto the data display canvas, its dialog box opens automatically, with the default data set tx selected.



- Select *Waveform.*
- Click the >> *Add* >> button.
- Click *OK.*

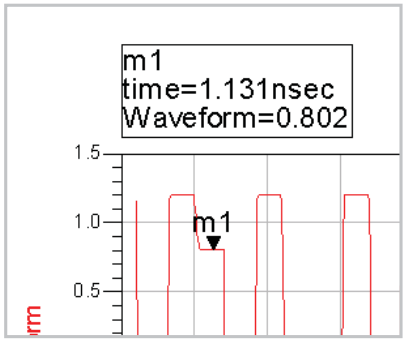
The plot appears. When a one follows a one or a zero follows a zero de-emphasis has been applied. Check the voltage.

- Click *Insert a New Marker* icon  .



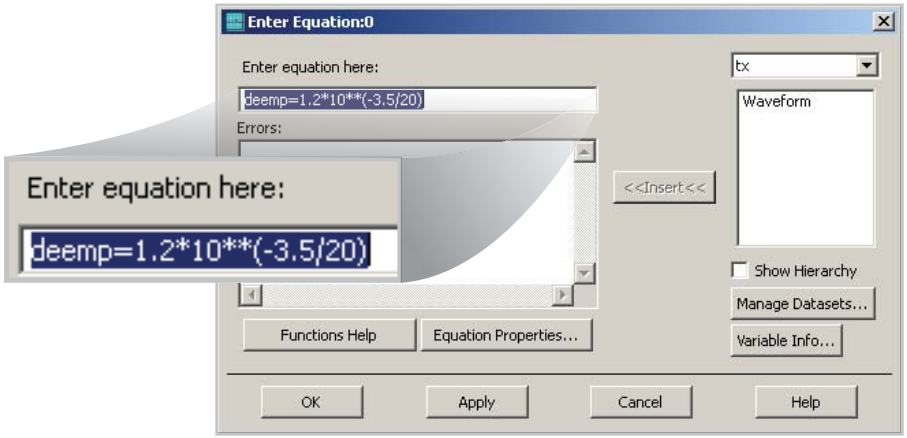
- Click on a one that follows a one:

The de-emphasis is 0.802 V. Data display equations are handy for all sorts of things including calculation of check values.



- In the palette, select *Eqn* 

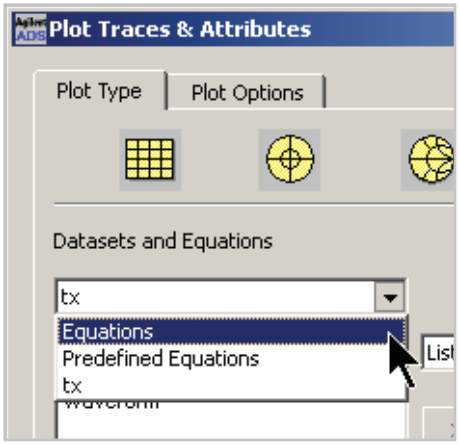
.
- Drop the equation onto the canvas.
- In its dialog box, enter the following equation:



- Click *OK.*
- In the palette, select *List* 

.

C: Data Display, DesignGuide Installation (Continued)



- Instead of the default dataset, select *Equations* from the drop down list.
- Select your deemp result and >> *Add* >> it.
- Click *OK*

As expected, the value agrees:

deemp
0.802

Congratulations!

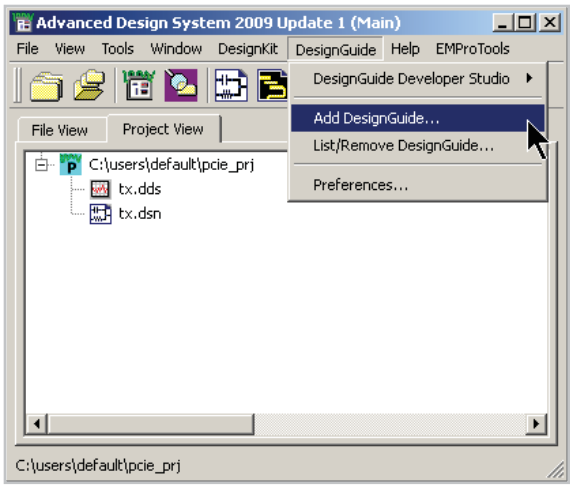
You completed the first simple "A B C" project.

We'll pick up the pace now by using one of ADS's powerful features: DesignGuides. These are pre-built project templates and tools. In our case, we'll use one that jump starts our PCI Express project.

- Login to our Knowledge Center and download the PCI Express Workshop DesignGuide from:

http://edocs.soco.agilent.com/display/eesofkc/PCIExpress

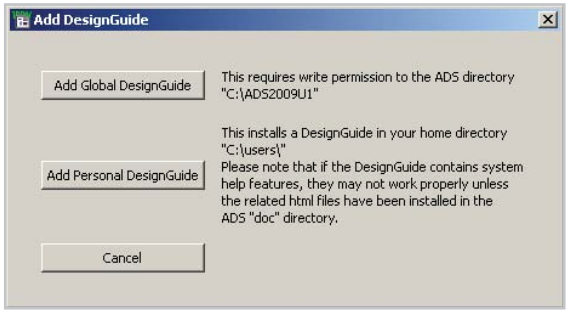
- Save it to your Desktop as 20090924_PCIExpress.deb .



- Select *DesignGuide* ► *Add DesignGuide...* from the main ADS window.
- You can add it as Personal or Global DesignGuide.
- Navigate to and select: 20090924_PCIExpress.deb.

You can manage your DesignGuides by selecting *DesignGuide* ► *List/Remove DesignGuide...*

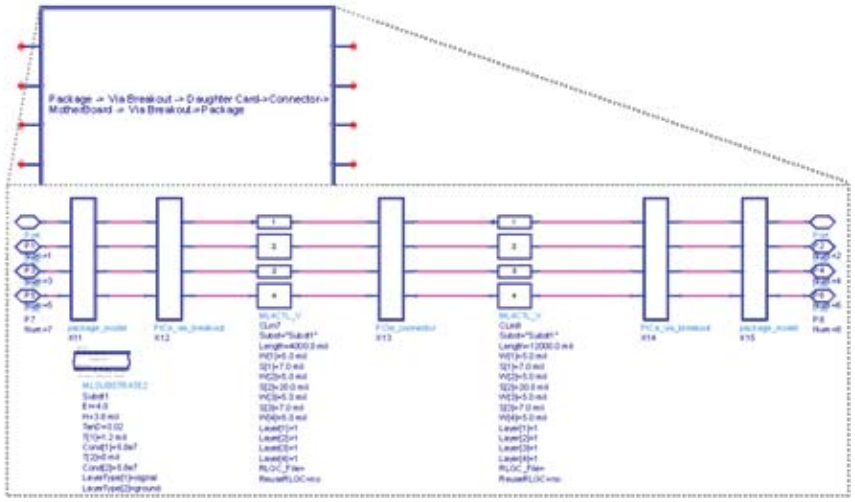
- Create a fresh schematic window, for example by clicking on  in the Main window.
- *Save As*... pcie.dsn.



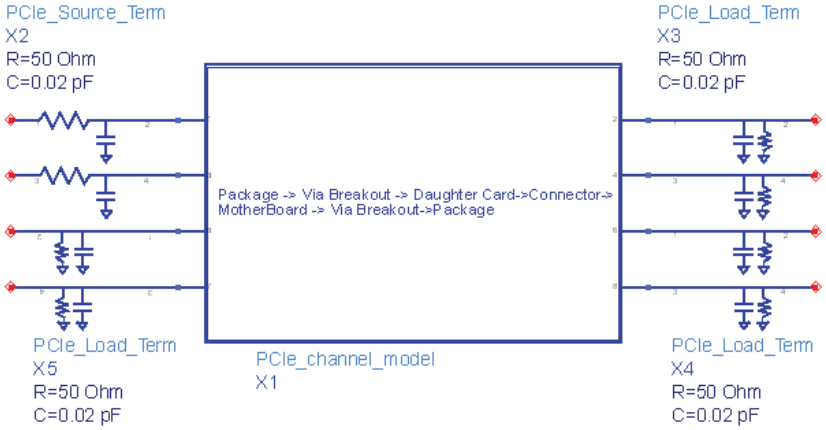
Determine Eye Diagram Performance for PCI Express Gen 2

We'll add source/load impedance, transmitter and eye probe to the pre-built DesignGuide PCI Express channel, then insert the receive mask and check for violations.

- On pcie.dsn place a PCI Express Channel model using the schematic's menu: *DesignGuide* ► *PCI Express* ► *PCI Express Interconnect Models* ► *Channel Model*.
- Use the tool bar icon Push and Pop icons  to explore the channel design hierarchy.



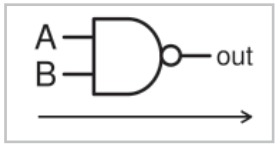
- Select the differential source termination: *DesignGuide* ► *PCI Express* ► *PCI Express Source/Load Terminations* ► *Source Impedance.*
- Connect it to the differential input pins.
- Select *Edit* ► *Move* ► *Move Component Text*, then click on a text block and move it if needed.
- Select the differential load termination: *DesignGuide* ► *PCI Express* ► *PCI Express Source/Load Terminations* ► *Load Impedance.*
- Connect three of them to other three differential pins:

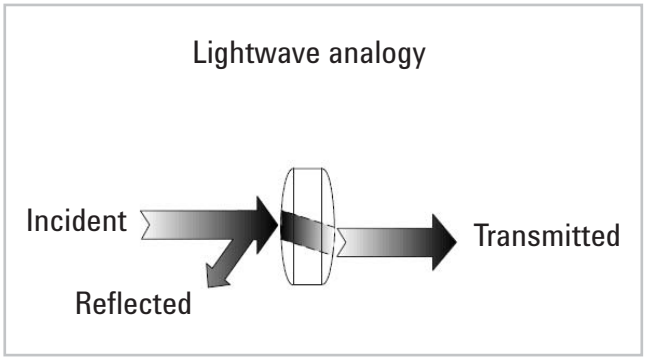


A Diversion Into S-Parameters

If you pushed into the hierarchy, you'd have noticed some components were defined using S-parameters. So let's take a short break from the keyboard and first say why we use network parameters in general, and S-parameters in particular, to characterize high frequency structures and components.

For low speed digital logic we only consider the forward propagation of signals, because, although reflections exists, they generally die down quickly if the interconnection flight time (propagation time) is short compared to the rise and fall times and the bit period. In fact, the incident signal or wave is partly transmitted and partly reflected:





Above figure: Agilent Application Note AN 1287-1, "Understanding the Fundamental Principles of Vector Network Analysis" http://cp.literature.agilent.com/litweb/pdf/5965-7707E.pdf

So, instead of a single transfer function, it might seem we now need two parameters to characterize a 2-port component at each frequency. In fact, the situation is more complex. The output port is also being bombarded with waves reflected off of the component in front of it in the cascade. These reverse waves are also partly transmitted (backwards down the cascade) and partly reflected off of the output port (heading back up the cascade). So we actually need four numbers per frequency point. Each is a complex number, representing magnitude and phase of the respective wave, relative the incident wave.

For reasons given below, it is convenient to collect the four numbers together in a two-by-two matrix called network parameters. There are several formats each of which have their pros and cons. The most convenient format for measurement purposes is the S-parameter format, because you can measure S-parameters using standard load, source, and connector impedances such as 50 ohms. In contrast, direct measurement of, say, Z parameters requires opens and short loads and sources, which are difficult to make at high frequencies and can damage some components. Once you have the S-parameters measured, there are simple calculations to convert to other formats if needed.

A Diversion into S-Parameters (continued)

For a 2-port network, the S-parameters are:

Description	Symbol
Desired transmission forwards of forward wave incident on input port	S21
Unwanted reflection backwards of forward wave incident on input port	S11
Unwanted transmission backwards of backward wave incident on output port.	S12
Unwanted reflection forwards of backward wave incident on output port	S22

The beauty of network parameters is that you don't have to sum an infinite series of partly reflected and partly transmitted waves bouncing up and down the cascade. The trick is that you can easily calculate the network parameters of arbitrary cascade of two-port components using a simple matrix calculation. All the internal reflections inside the newly created "black box" can be ignored, and the cascade treated as a composite two-port network, characterized by only four parameters per frequency point.

Network parameters can be generalized to more than two-ports and more than simple cascade connection. Here we'll use a 4 X 4 matrix S-parameters to represent a four-port network: a pair of coupled transmission lines such as those used in a differential interconnect.

One of the things ADS does really well is convert frequency domain S-parameters into a time-domain model. Other tools often leave you with an incorrect non-causal or non-passive conversion.

For more information on S-parameters, please see *Agilent Application Note AN 95-1, S-Parameter Techniques for Faster, More Accurate Network Design,* by Richard W. Anderson, available in two formats:

- Slides plus interactive features:
  http://contact.tm.agilent.com/Agilent/tmo/an-95-1/index.html?cmpid=34689
- Scan of the classic 1967 article:
  http://cp.literature.agilent.com/litweb/pdf/5952-1130.pdf

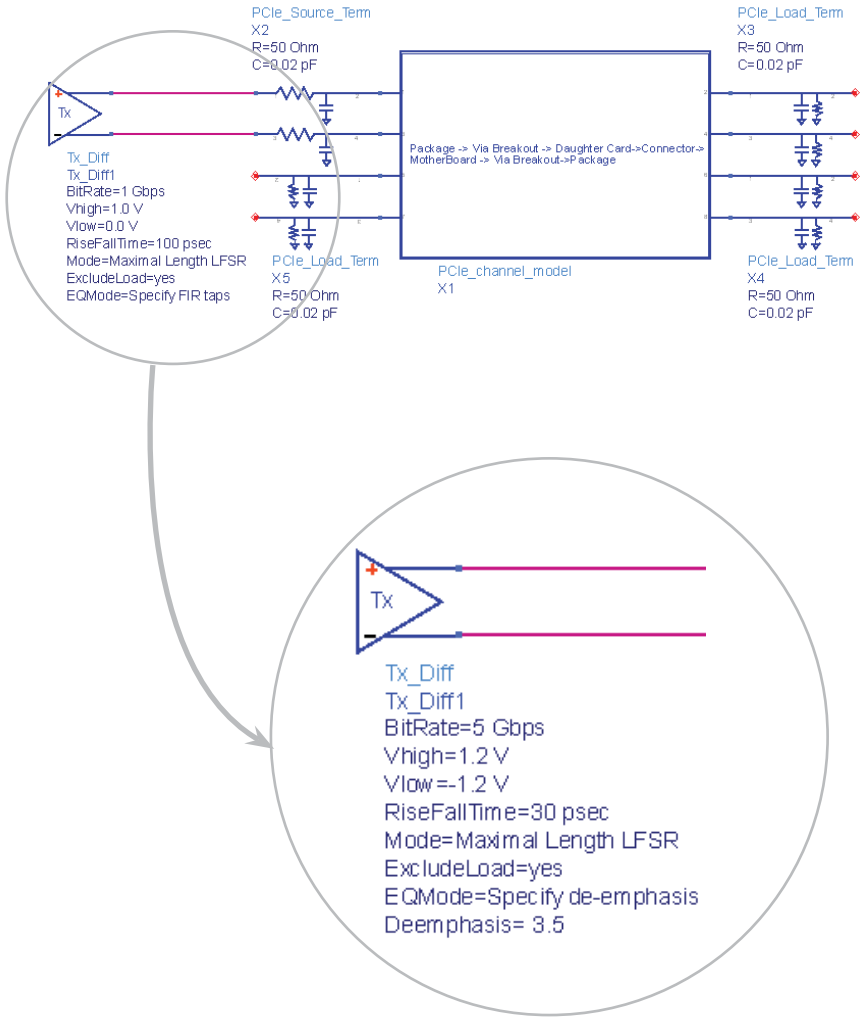
Now let's return to our PCI Express project...

Add the Transmitter

From the *Simulation–ChannelSim* palette:

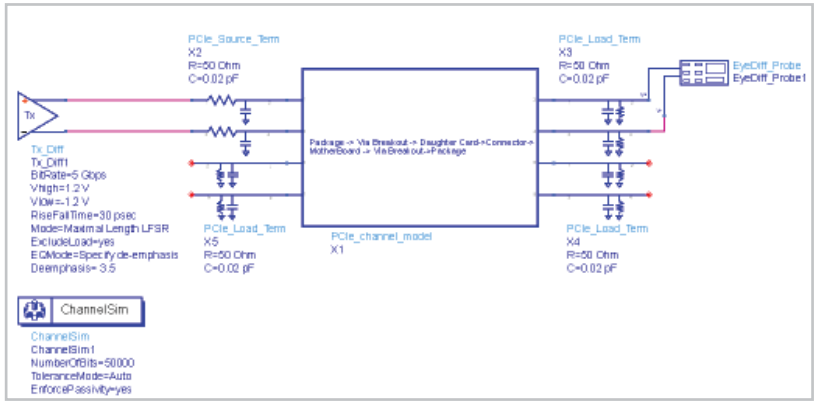
- Select *Tx_Diff.*
- Connect it to the input differential pins.
- Double click on *Tx_Diff1* instance.
- Go to the appropriate tabs to edit the following parameters:

PRBS ▶ Bit rate	5 Gbps
PRBS ▶ Vhigh	1.2 V
PRBS ▶ Vlow	–1.2 V
PRBS ▶ Rise/Fall	30 ps
PRBS ▶ Register Length	23
Encoder ▶ 8B10B	Enable
EQ ▶ Specify de-emphasis	3.5 dB



Add Eye Probe and Simulation Controller

- Select the *EyeDiff_Probe* from the same palette and connect it to the differential output pins.
- Place a Channel Simulation Controller (*ChannelSim*) on the schematic page.
- Set the *ChannelSim1* parameter *NumberOfBits* to 50000.

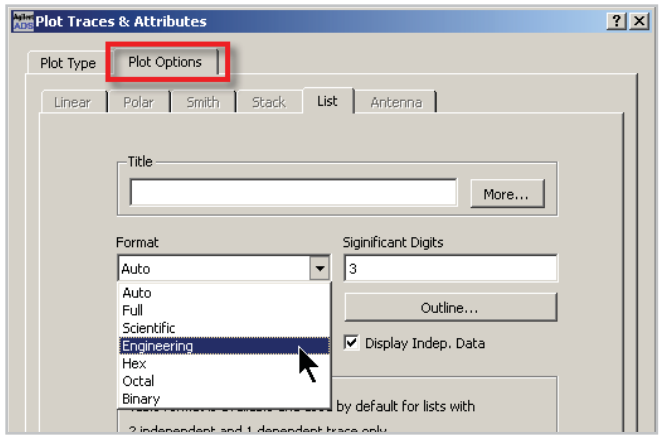


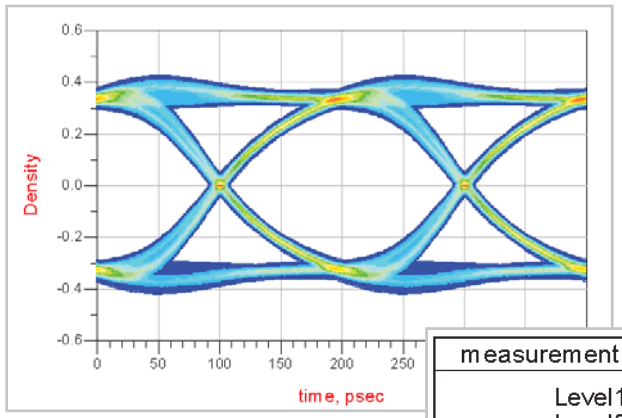
- Click in the *Simulate* tool bar icon:  .

A new data display window opens.

- Save the data display as pcie.dds.
- Place a rectangular plot and add the *Density* trace from the default pcie data set.
- Place a List and add *Summary* measurements.

- Select the Plot Options tab.
- Select *Format* ▶ *Engineering*.
- Click *OK*.



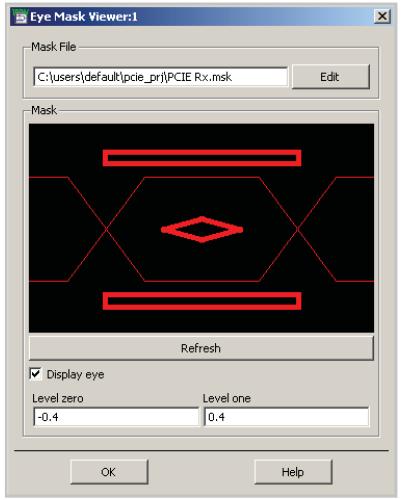


measurement	Summary
Level1	334.4 m
Level0	-323.5 m
Height	546.0 m
Width	183.0 p
MaskViolated	0.0000

Add an Eye Mask, Check for Mask Violation

- Go back to the pcie.dsn schematic.
- *Copy the receive mask file to current project directory by selecting: DesignGuide ► PCI Express ► PCI Express Mask ► PCI Express Receive Mask.*
- Double click on *EyeDiff_Probe1*.
- In its dialog box (*Parameters* tab), set the *Use Eye Mask* check box.
- Click *Browse*.
- Navigate to PCIE Rx.msk and click *Open*.
- Click the *View/Edit* button.
- Set *Level zero* to -0.4 and *Level one* to 0.4.
- Click *Refresh*.
- Click Edit.

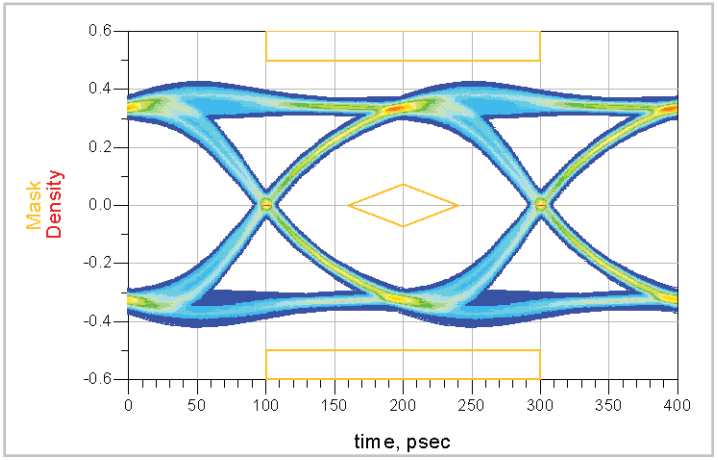
A text editor opens, showing the mask file. You can edit or create these files to suit. The format is the same as those for Agilent oscilloscopes.



- Dismiss the text editor.
- Dismiss the Eye Mask Viewer dialog box.
- From the Measurements tab, *Click the >> Add >> button to add EyeMaskViolation measurement*.
- Click *OK* to dismiss the *EyeDiff_Probe1* dialog.
- *Simulate*  .
- In the pcie data display, double click on the frame of the density plot to open its dialog box.
- *Click the >> Add >> button to add the Mask data*.

You can double click on any trace and set the thickness, color, etc. from the *Trace Options* ► *Trace Options* tab.

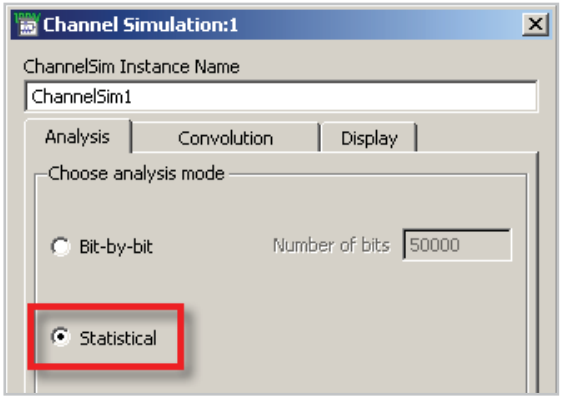
measurement	Summary
Level1	334.4 m
Level0	-323.5 m
Height	546.0 m
Width	183.0 p
MaskViolated	0.0000



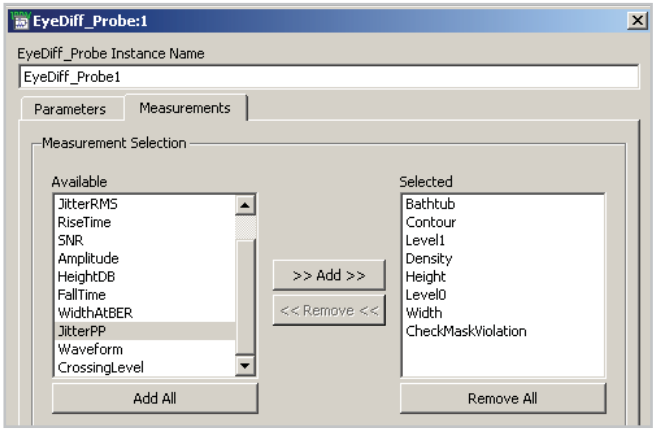
A *MaskViolated* value of 0 (false) indicates no mask violation.

BER Contours Using Statistical Mode of Channel Simulator

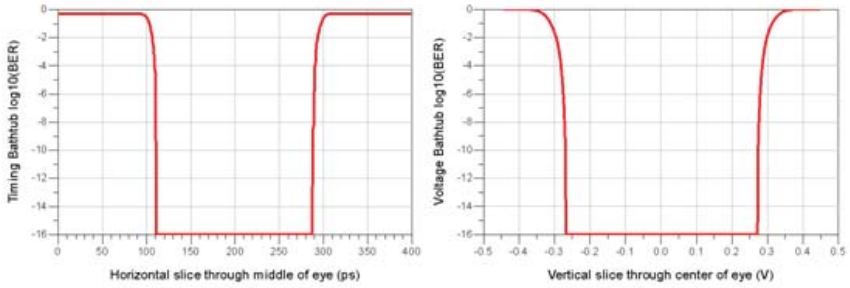
- Go back to the pcie schematic.
- Choose *Statistical* instead of *Bit-by-bit* mode from *ChannelSim1* ▶ *Analysis* tab.



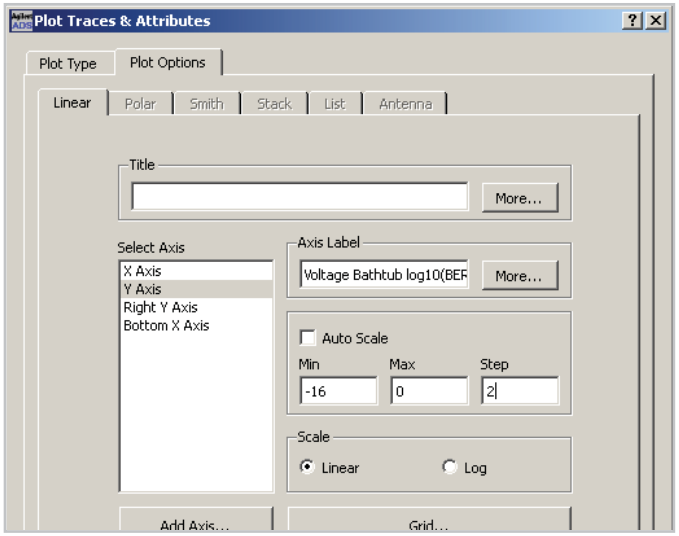
- >> *Add* >> Bathtub and Contour using the *EyeDiff_Probe1* ▶ *Measurements* tab.



- *Simulate*  .
- In the data display density plot, >> *Add* >> *Contour.*
- In rectangular plots, plot *VoltageBathtub* and, separately, *TimingBathtub*.



- Customize the *Title* of the plot and the *Min*, *Max*, *Step*, and *Label* of its axes from the *Plot Options* tab.



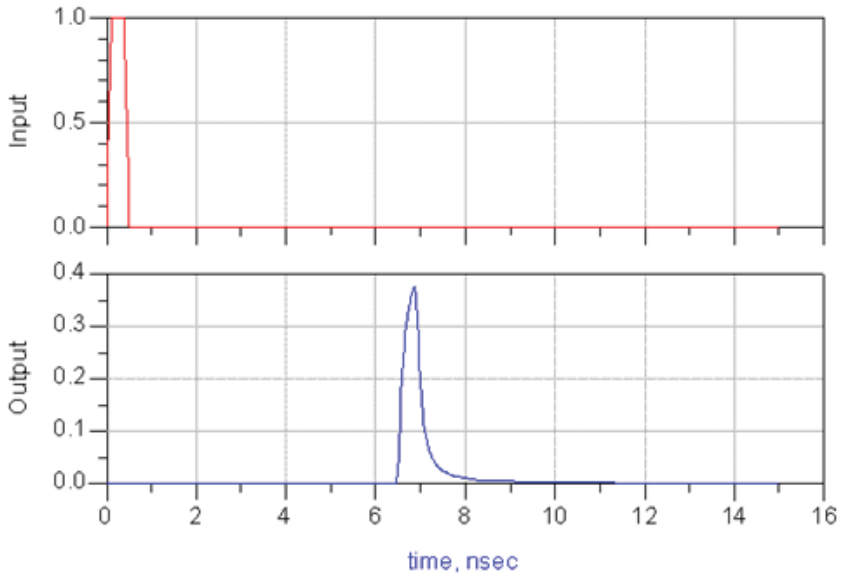
Channel Simulator: Bit-by-Bit Mode

By now you might be asking, "What's the difference between traditional transient (SPICE-like) simulation and the two modes of Channel Simulator?"

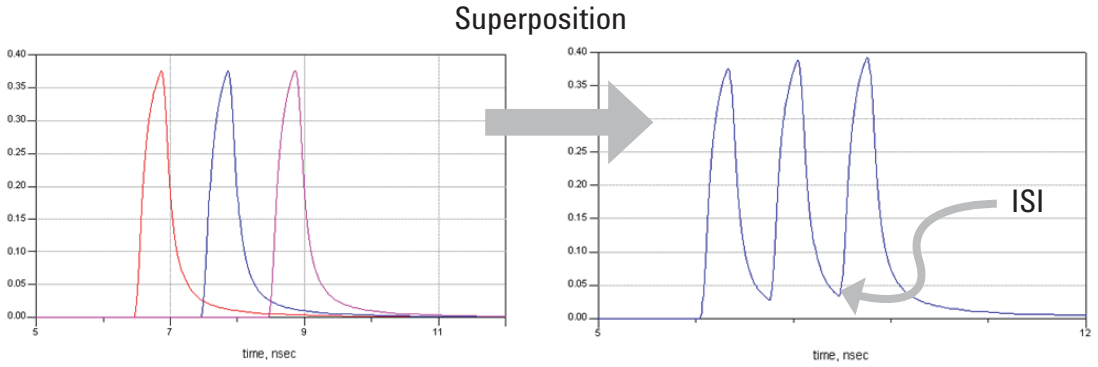
Bit-by-bit mode works in two phases. First, we probe your schematic with single step input. We use transient simulator but we also automatically use convolution (to deal with any components defined in the frequency domain) and EM simulators (to deal with distributed or layout components). The (computationally expensive) transient simulation need run only for a short length of time, equal to the pulse response also called the channel memory.

In phase two we use the step response from phase one as a linear time invariant model. We use (computationally inexpensive) superposition to calculate the output for millions of bit without having to call the transient, convolution, or EM simulators again.

Phase 1: SPICE-like transient response of single step – runs on existing schematic.



Phase 2: Million-bit-per-minute throughput using superposition

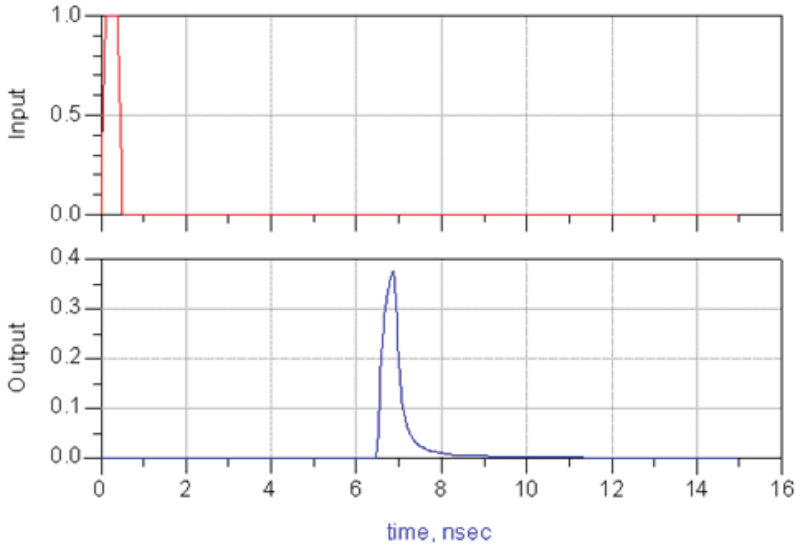


Channel Simulator: Statistical Mode

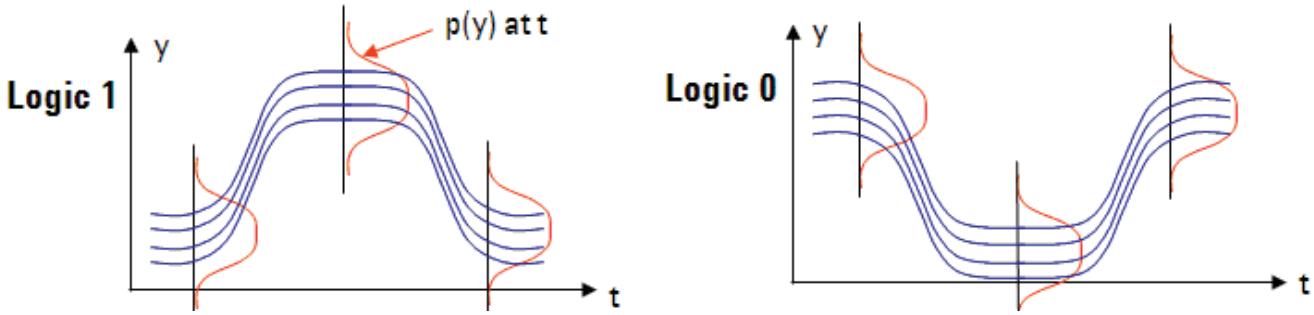
In statistical mode, again we have two phases. The first phase is the same as for bit-by-bit mode, but the second step is much quicker. There's no need for brute force superposition of each bit: just some calculations based on:

- ISI and crosstalk implied in the through and crosstalk pulse responses
- Jitter spec
- Equalizer spec
- Line coding

Phase 1: SPICE-like transient response of single step – runs on existing schematic



Phase 2: Statistical calculations including ISI, crosstalk, jitter specification, equalizers, and encoding



Comparison of Techniques

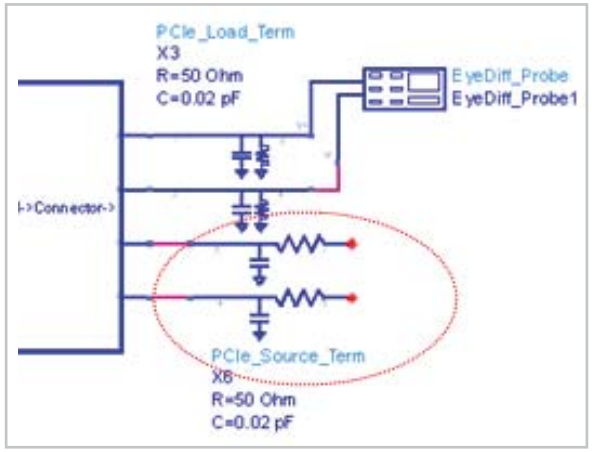
This table compares the three techniques.

	Transient (SPICE-like) Simulator	Channel Simulator, Bit-by-bit mode	Channel Simulator, Statistical mode
Method	Modified nodal analysis of Kirchoff's current laws for every time step	Bit-by-bit superposition of step responses	Statistical calculations based on step response
Applicability	Any circuit	LTI channel; finite, user-specified bit pattern; adaptive or fixed eq. taps	LTI channel; stochastic props of infinite bit pattern; fixed eq. taps
BER floor in one minute simulation	$\sim 10^{-3}$	$\sim 10^{-6}$	$\sim 10^{-16}$

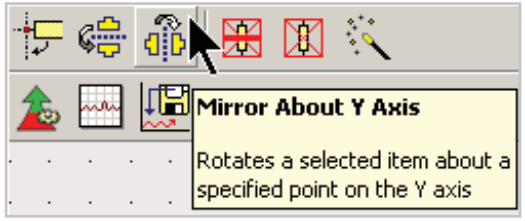
Now, back to our project...

Modeling Crosstalk,Comparing Two Simulations

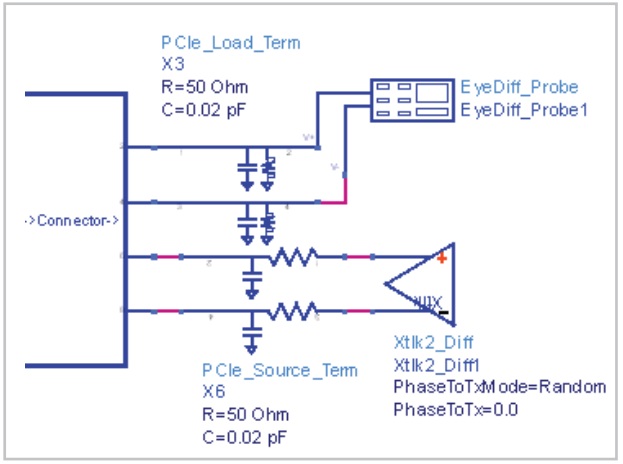
- *Save*  the pcie schematic file.
- Delete the load termination at the far end of the crosstalk channel (FEXT).
- Replace it with source termination.



- From the Channel Simulator Palette, select the *Xtlk2_Diff* transmitter.
- Click *Mirror About Y Axis* to flip the ghost cursor.



- Connect it to the FEXT source termination.



Channel Simulator requires exactly one *Tx* component, but you can add as many *Xtlk2_Diff* aggressors as you need.

- Select the *Random* radio button of the *Phase Relative to Tx* setting of *Xtlk2_Diff1* ► *PRBS*.

We'll compare results with and without FEXT by saving the modified version with a different name.

- From the schematic menu select *File* ► *Save Design As...* and enter pcie_fext.dsn.
- *Simulate*  .

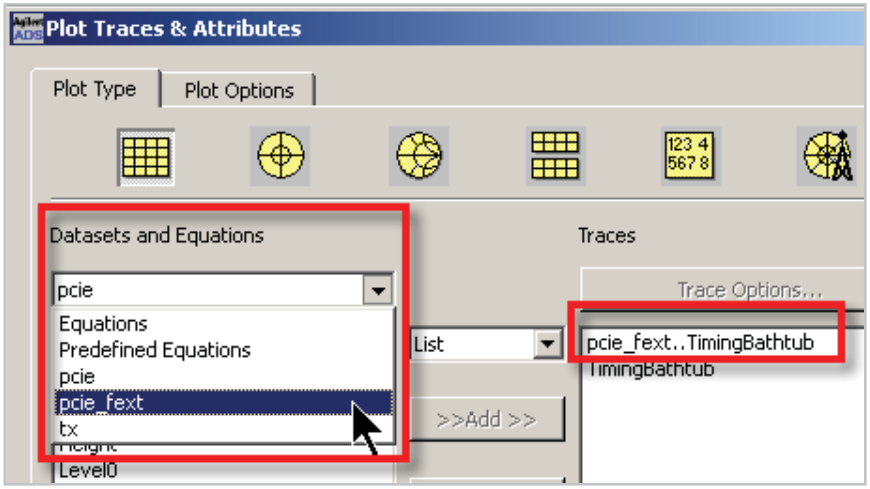
A new, blank data display window opens, but we want to re-use the previous one, so:

- Close pcie_fext.dds .
- Go to your previous data display window.

Compare Simulation With and Without Crosstalk

You can compare corresponding traces from two different datasets by using their full names. These have the format: dataset..trace (trace alone is just a shorthand for that item in the default dataset).

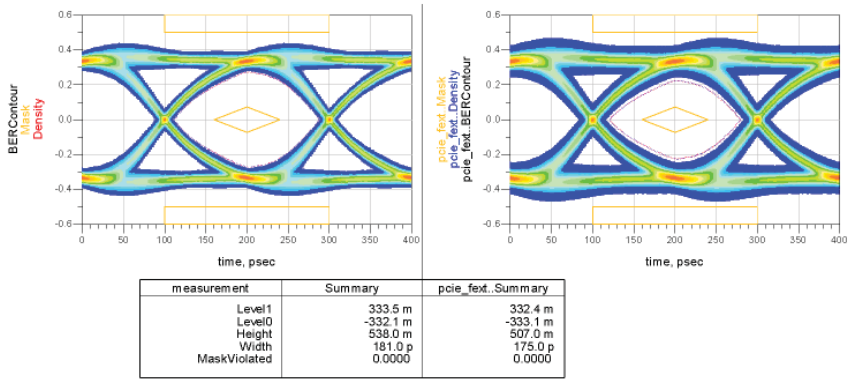
- Double click on the timing bathtub plot.
- Select pcie_fext, then add *TimingBathtub*:
- Similarly, add *VoltageBathtub* to that plot, and Summary to the



List plot.

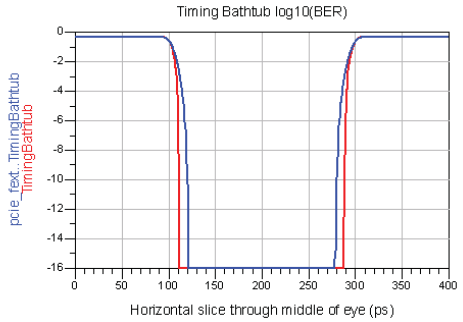
Overlaying two density and two contour traces on one plot is possible but messy, so:

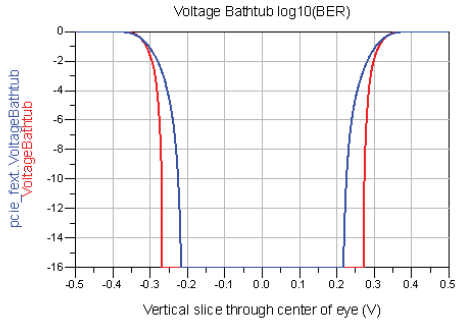
- Create a separate density and contour plot for the new data set.



measurement	Summary	pcie_fext..Summary
Level1	333.5 m	332.4 m
Level0	-332.1 m	-333.1 m
Height	538.0 m	507.0 m
Width	181.0 p	175.0 p
MaskViolated	0.0000	0.0000

The eye height and width are reduced by FEXT, but the mask isn't violated.

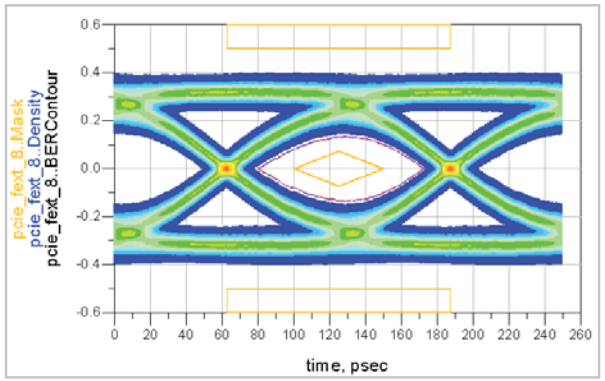




Let's see if we can push this design to a higher bit rate...

Explore the Design Space at 8 Gigabits per Second: Equalization

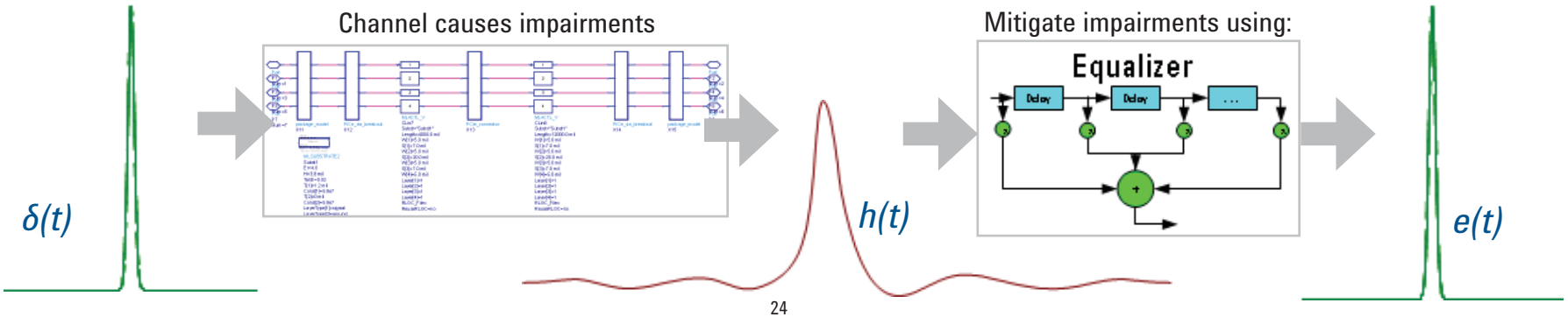
- *Save*  the 5 Gbps version of the schematic.
- Change the data rate of *Tx_Diff1* and *EyeDiff_Probe1* to 8 Gbps.
- *File* ► *Save Design As...* and enter pcie_fext_8.
- *Simulate*  .
- Compare the eye diagram as we did before.



The mask still isn't violated at our selected 10^{-12} BER contour, but it's getting close. How can we improve our margin? The channel impairs the signal by acting like a low pass filter, and introducing echo-like reflections. These smear out the impulse response.

We can add an equalizer at the receive end that mitigates these impairments. An equalizer is simply a filter whose response is the inverse of the channel response.

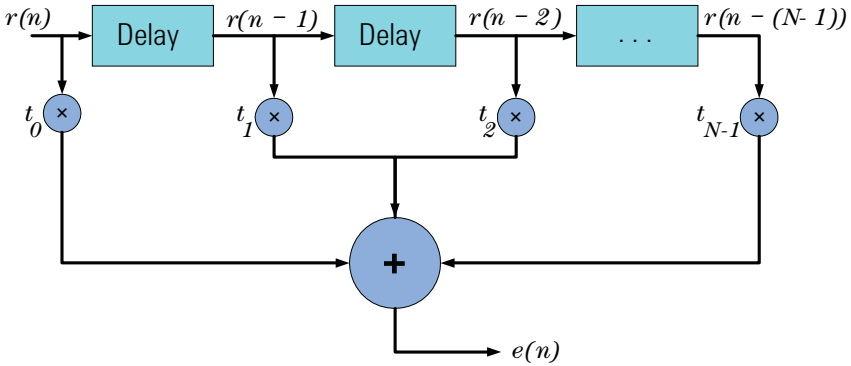
Mitigate channel impairments with an equalizer



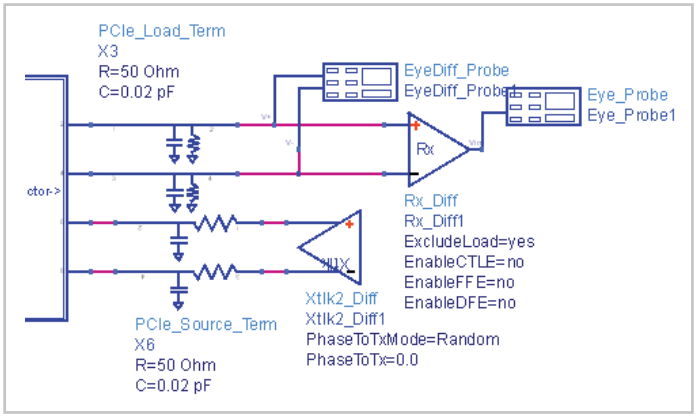
Add a Feed Forward Equalizer (FFE)

For the Feed Forward Equalizer, we define the n^{th} received sample as *r(n)*, and the N^{th} tap coefficient as t(N), then the n^{th} output sample *e(n)* is:

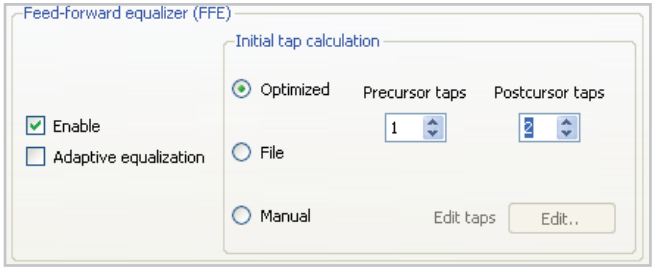
$$e(n) = \sum_{k=0}^{N-1} t(k)\, r(n-k)$$



- Save  the 8 Gbps version of the schematic.
- From the *Simulation-ChanSim* palette, select and place an *Rx_Diff* component.
- Add a single-ended eye probe like so:



- Edit *Rx_Diff1* and *Enable* the FFE with *Initial tap calculations* as *Optimized*, number of *Pre-cursor taps* as 1 and *Post cursor taps* as 2.



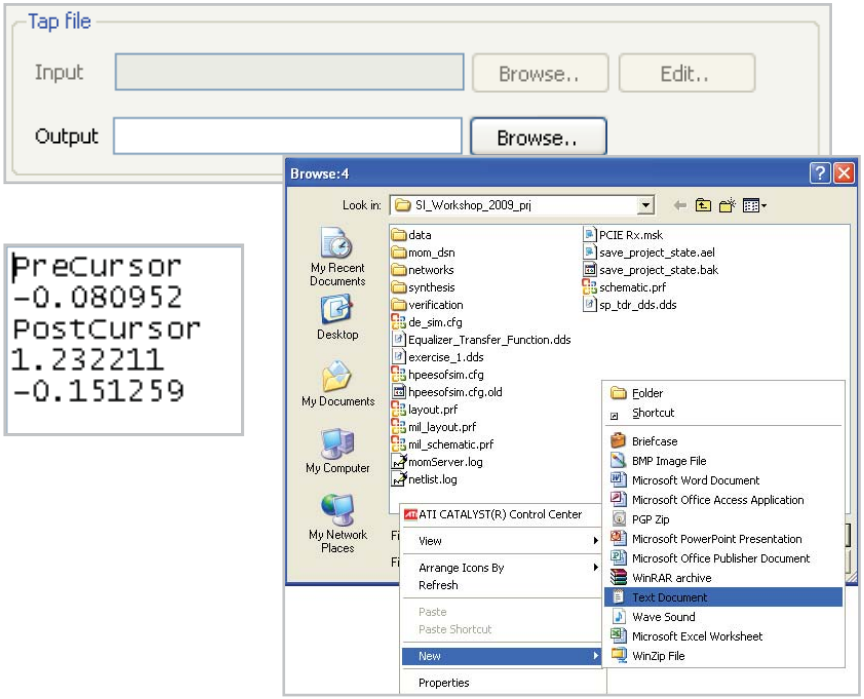
- *File* ► *Save Design As...* and enter pcie_lfe.
- Simulate.

Equalization Results, Next Steps

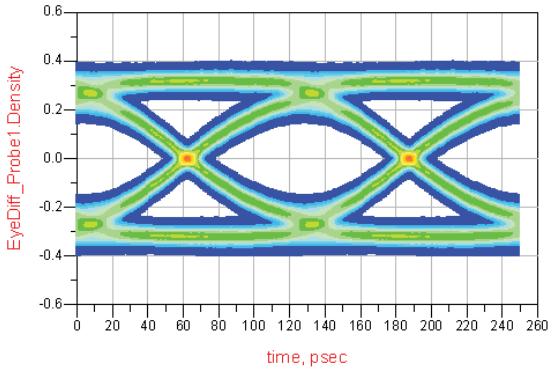
- Plot eye diagram before equalization and after equalization.

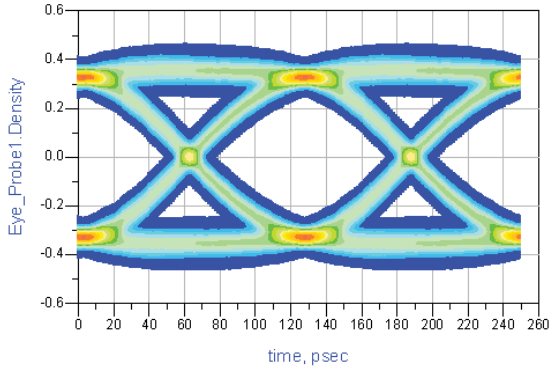
The receiver component has automatically calculated the optimized tap coefficient values. You can output optimized tap coefficients:

- Double click on *Rx_Diff1* and select Edit... ► Output ► Browse.
- In the *Browse* window, using right mouse click create a new file taps.txt .
- Re-simulate the design and open taps.txt file to look at the taps coefficients.




```
PreCursor
-0.080952
PostCursor
1.232211
-0.151259
```





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